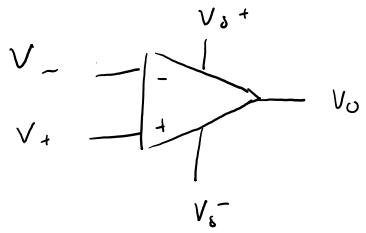
Operational Amplifiers

Tuesday, January 4, 2022 3:43 PM

Def OpAmps are general purpose voltage amplifiers



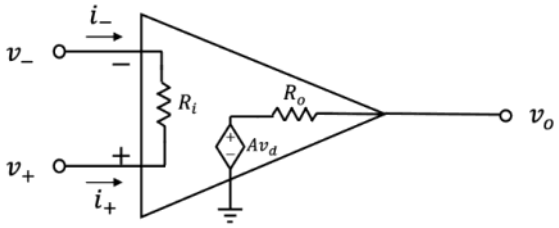
cncl: $V_s^- < V_o < V_s^+$

$$V_o = A(V_+ - V_-) = A v_d$$

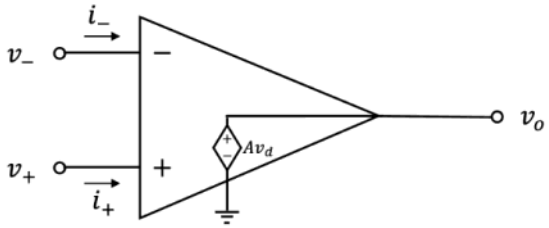
where A is the open loop voltage gain

Def

Linear model



Ideal model



Open Loop Operation, Feedback

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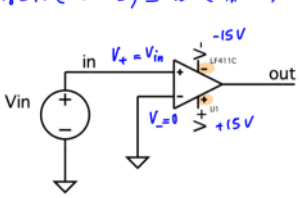
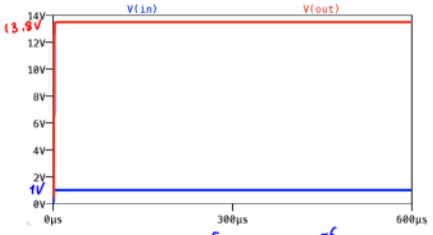
Open-loop operation of op-amps (no feedback)

$A = 10^5$

$V_o = A(V_+ - V_-) = 10^5 (V_{in} - 0) = 10^5 \times V_{in}$





$V_{omax} = 13.8\,V$, here.

$V_o = 10^5 V_{in} \rightarrow V_{in\,max} = \frac{V_{omax}}{10^5} = \frac{13.8\,V}{10^5} = 13.8 \times 10^{-5} = 138 \times 10^{-6}\,V = 138\,\mu V$

In open-loop configuration, op-amp cannot amplify input voltages greater than a few micro volts. It cannot be used as a voltage amplifier.

$V_{omax} = 13.8\,V$ and $A = 10^5$,

since $V_o = A \cdot V_{in}$ then:

$V_{omax} = 10^5 V_{in\,max}$

$13.8\,V = 10^5 \cdot V_{in\,max}$

$V_{in\,max} = \frac{13.8\,V}{10^5} = 138\,\mu V$

which is very small

Thus it is not an effective amplifier

Def Feedback: portion of output is feed back into the input

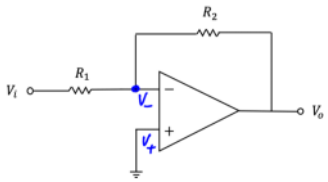
Negative feedback: In circuits with negative feedback, as the output increases, the input will decrease, and vice versa, such that the output signal would reach the desired stable level.

Positive feedback: In circuits with positive feedback, when the output increases, the input will also increase, and vice versa. The output of circuits with positive feedback is always at its limits.

$V_o = A V_d$

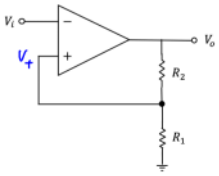
$V_d = V_+ - V_-$

$V_- = \frac{R_2}{R_1+R_2} V_i + \frac{R_1}{R_1+R_2} V_o$



$V_+ = \frac{R_1}{R_1+R_2} V_o$

$V_o = A(V_+ - V_-) = A(V_+ - V_i)$



In General: $\frac{V_o}{V_i} = -\frac{R_2}{R_1} \cdot \frac{1}{1 + \frac{1}{AB}}$

$B = \frac{R_1}{R_1+R_2}$

Virtual Short Principle: V_o is a finite value:

$V_o = A v_d \rightarrow v_d = \frac{V_o}{A} \approx 0$

$V_+ \approx V_-$

then: $\frac{V_o}{V_i} = -\frac{R_1}{R_2}$

Limitations

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Saturation: since $V_S^- \leq V_o \leq V_S^+$, the output is limited by the power supply voltage.

Current: op-amps have a maximum output current.

Semiconductors (P-type, N-type)

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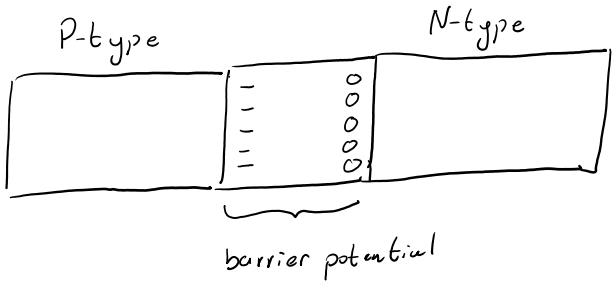
N-type semiconductors: doped with group 5 elements - has extra electrons

P-type semiconductors: doped with group 3 elements - has extra holes

both N-type and P-type are electrically neutral

In a P-N junction diode, a P-type and N-type are connected.



when (+) voltage and (-) voltage are applied to the P-type and N-type then it is forward biased

the opposite is backward biased

Idea During forward biasing, the width of the barrier potential decreases until the whole diode conducts a current.

During reverse biasing, the width of the barrier potential widens and only some small reverse current is conducted.

Diodes

Sunday, January 9, 2022 5:27 PM

Symbol: 

IV characteristic (piecewise): when diode is off: $I_D = 0$, $V_D < V_T$

when diode is on: $I_D \geq 0$, $V_D = V_T$

Solving: assume either the diode is off or on, and solve for V_D to either verify the assumption or reject the assumption.

Steps:

1) assume diode is off
2) find V_D, if $V_D < V_T$, diode is off
3) assume diode is on
4) $V_D = V_T$, find I_D, if $I_D \geq 0$ then diode is on, otherwise off

LEDs, Zener Diodes

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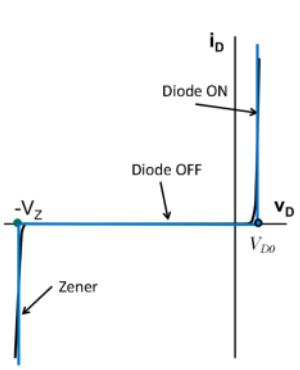
LED: Larger band gap, $V_T \approx 1.7V - 1.9V$

Zener Diode: Typical diode IV for forward bias, when $V_D \geq V_T$, $V_D = V_T$, $I_D \geq 0$

Allows current to flow in reverse bias in reverse direction

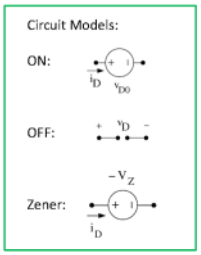
IV characteristic:



Diode ON: $v_D = V_{D0}$ and $i_D \geq 0$

Diode OFF: $i_D = 0$ and $-V_Z < v_D < V_{D0}$

Zener: $v_D = -V_Z$ and $i_D \leq 0$



ON: $V_D = V_T$, $I_D \geq 0$

OFF: $V_Z < V_D < V_T$, $I = 0$

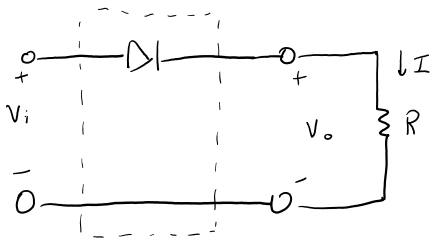
Zener: $V_D = -V_Z$, $I_D \leq 0$

Symbol:

Diode Waveform Shaping Circuits

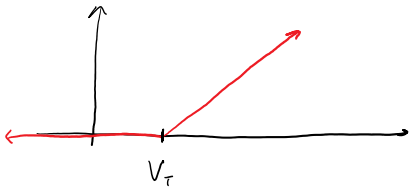
Thursday, January 13, 2022 7:31 PM

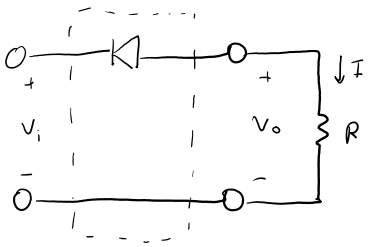
1) Rectifier Circuits:



when $V_i < V_T$, $V_o = 0$

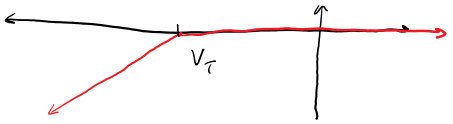
when $V_i \geq V_T$, $V_o = V_i - V_T$



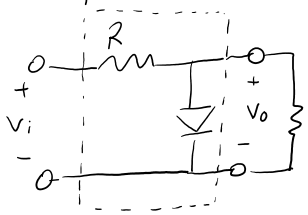


when $V_i > V_T$, $V_o = 0$

when $V_i \leq V_T$, $V_o = V_i + V_T$

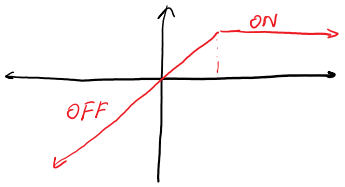


2) Clipper Circuit:

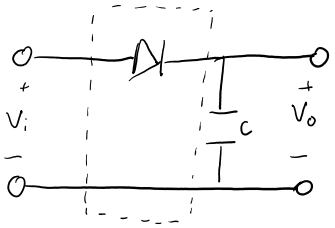


when $V_i < V_T$, $V_o = V_i$

when $V_i \geq V_T$, $V_o = V_T$



3) Peak Detector Circuits:

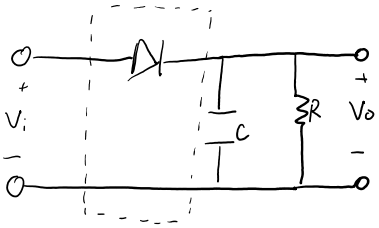


when $V_i < V_c + V_T$, $V_D < V_T$, $I_D = 0$ and $V_o = V_c$

when $V_i \geq V_c + V_T$, $V_D = V_T$, $I_D \geq 0$ and $V_c = V_i - V_D$

Ideally, the capacitor does not discharge, so V_c stays constant after every peak.

In practice, there is always a resistor in parallel:

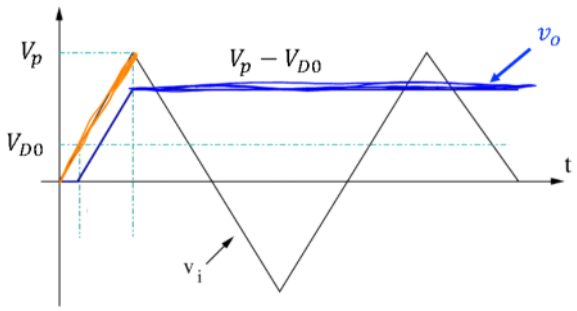


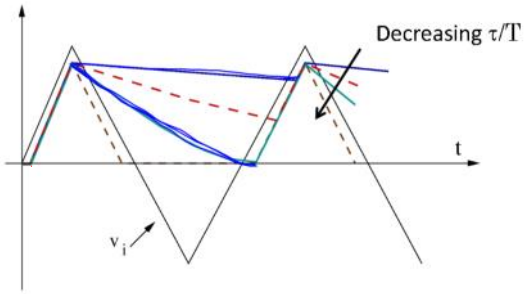
when $V_i < V_c + V_T$, $V_D < V_T$, $I_D = 0$

and $V_c = V_c e^{-(t - t_0)/\tau}$ where $\tau = RC$

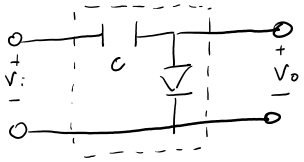
when $V_i \geq V_c + V_T$, $V_D = V_T$, $I_D \geq 0$ and $V_C = V_i - V_D$

Ideal case: Does not decrease over time Practical case: Decreases at rate $e^{-(t-t_0)/\tau}$





4) Clamp Circuits:

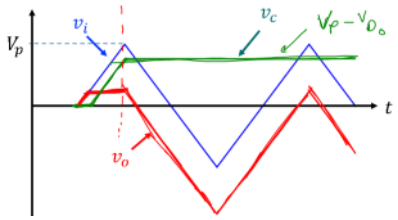


In general: $V_o = V_i - (V_p - V_T)$

Always: $V_o = V_i - V_c$ where $V_c = V_p - V_T$

Without Load:

The diode turns OFF when the capacitor is charged to $v_c = V_p - V_{D0}$

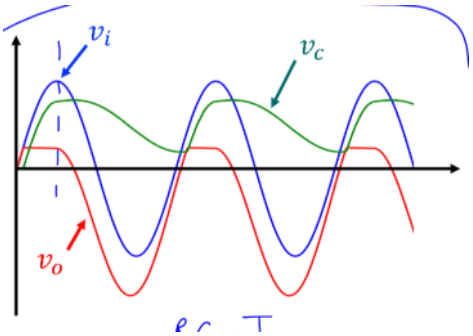


$v_o = v_D = v_i - v_c$

Diode off:

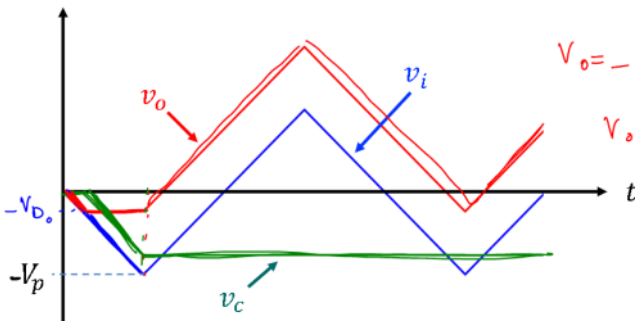
$v_o = v_i - (V_p - V_{D0})$

With Load:



To solve: solve for the peak detector, $V_o = V_i - V_c$

By reversing the diode and voltage source, we can shift positively:



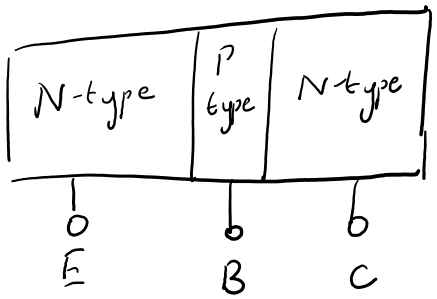
Reverse: V_c charges to $-(V_p - V_T)$

$V_o = V_i - V_c = V_i + (V_p - V_T)$

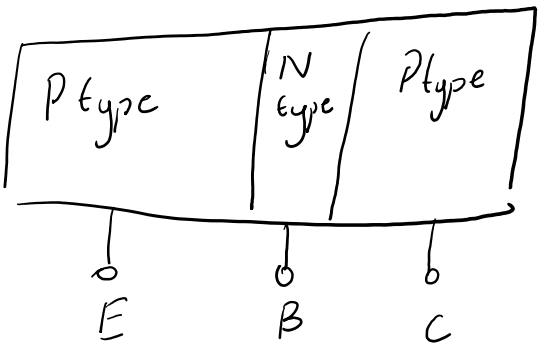
BJT (Bipolar Junction Transistor)

Thursday, January 27, 2022 5:02 PM

NPN :



PNP :



Construction: • Thin base region (between E & C)

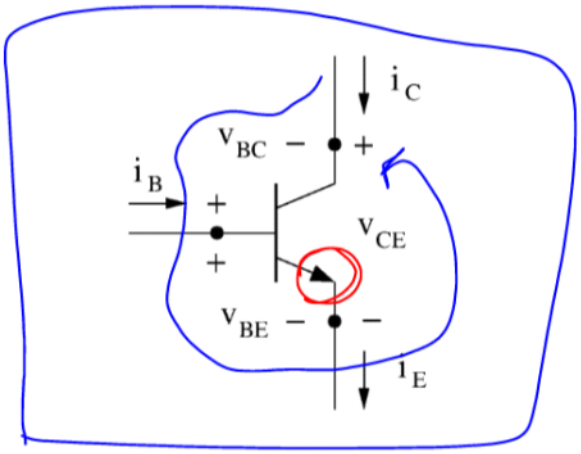
• Heavily doped emitter

• Large area collector

Symbol and IV Characteristics

Thursday, January 27, 2022 5:06 PM

NPN transistor



Circuit symbol and Convention for current directions

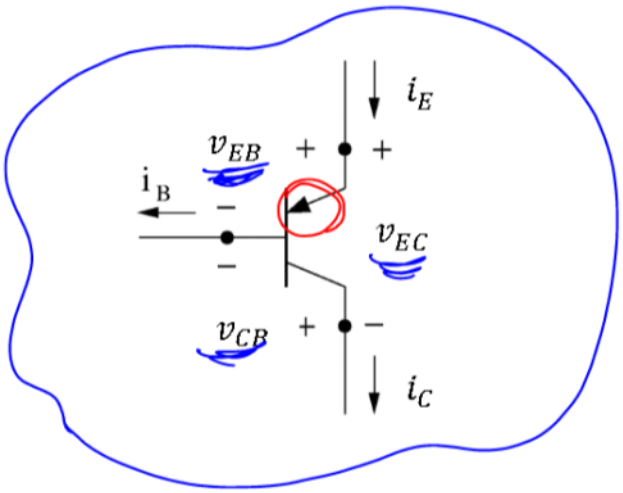
KCL: $i_E = i_C + i_B$

KVL: $v_{BC} = v_{BE} - v_{CE}$

Note:

$$v_{CE} = v_C - v_E$$

PNP transistor



KCL: $i_E = i_C + i_B$

KVL: $v_{CB} = v_{EB} - v_{EC}$

Note:

$$v_{EC} = v_E - v_C$$

BJT Operation Modes

Thursday, January 27, 2022 5:12 PM

When BJT is in cutoff mode:

$I_B = 0, \quad I_C = 0 \qquad I_E = 0$

When BJT is in active mode:

$I_B \geq 0 \qquad V_{BE} = V_{DO} \qquad I_C = \beta \cdot I_B \qquad V_{CE} \geq V_{DO}$

When BJT is in saturation mode:

$I_B \geq 0 \qquad V_{BE} = V_{DO} \qquad I_C < \beta I_B \qquad V_{CE} = V_{sat}$

where β is the current gain of the BJT

Note: For Si based BJT, if V_{DO} is not given, $V_{DO} = 0.7\ V$

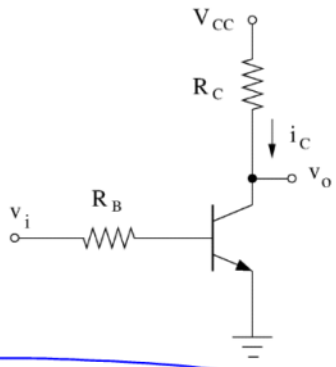
BJT Transfer Functions

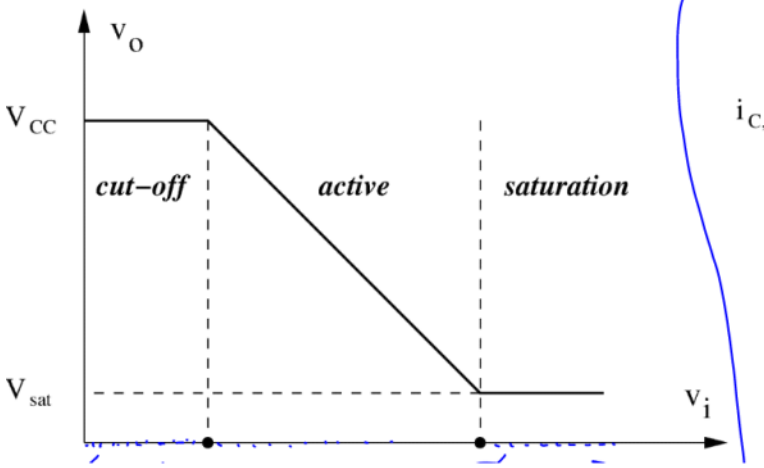
Tuesday, February 1, 2022 5:35 PM

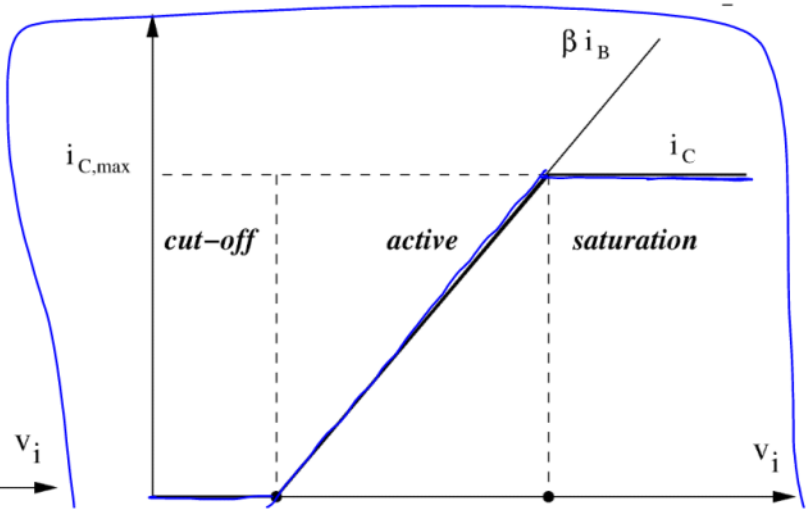
$$v_i < V_{D0} \rightarrow \text{BJT in Cutoff}$$

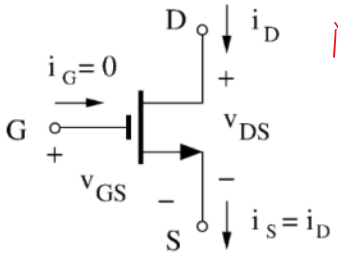
$$V_{D0} \le v_i \le V_{D0} + \frac{V_{CC} - V_{D0}}{\beta R_C / R_B} \rightarrow \text{BJT in active}$$

$$V_{D0} + \frac{V_{CC} - V_{sat}}{\beta R_C / R_B} < v_i \rightarrow \text{BJT in deep saturation}$$

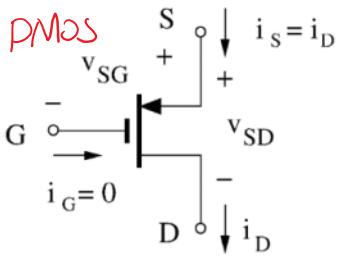








MOS i-v Equations



NMOS $(V_{OV} = v_{GS} - V_{tn})$

Cut– Off :	$V_{OV} < 0$	$i_D = 0$
Triode :	$V_{OV} \geq 0$ and $v_{DS} \leq V_{OV}$	$i_D = 0.5\,\mu_n C_{ox} \frac{W}{L}(2\,V_{OV} v_{DS} - v_{DS}^2)$
Saturation :	$V_{OV} \geq 0$ and $v_{DS} \geq V_{OV}$	$i_D = 0.5\,\mu_n C_{ox} \frac{W}{L} V_{OV}^2\,(1 + \lambda v_{DS})$

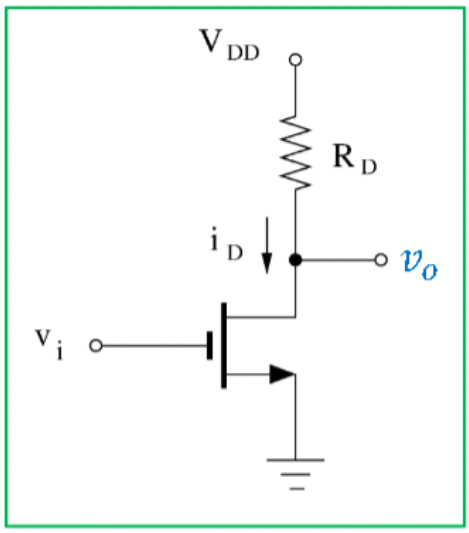
PMOS $(V_{OV} = v_{SG} - |V_{tp}|)$

Cut– Off :	$V_{OV} < 0$	$i_D = 0$
Triode :	$V_{OV} \geq 0$ and $v_{SD} \leq V_{OV}$	$i_D = 0.5\,\mu_p C_{ox} \frac{W}{L}(2\,V_{OV} v_{SD} - v_{SD}^2)$
Saturation :	$V_{OV} \geq 0$ and $v_{SD} \geq V_{OV}$	$i_D = 0.5\,\mu_p C_{ox} \frac{W}{L} V_{OV}^2\,(1 + \lambda v_{SD})$

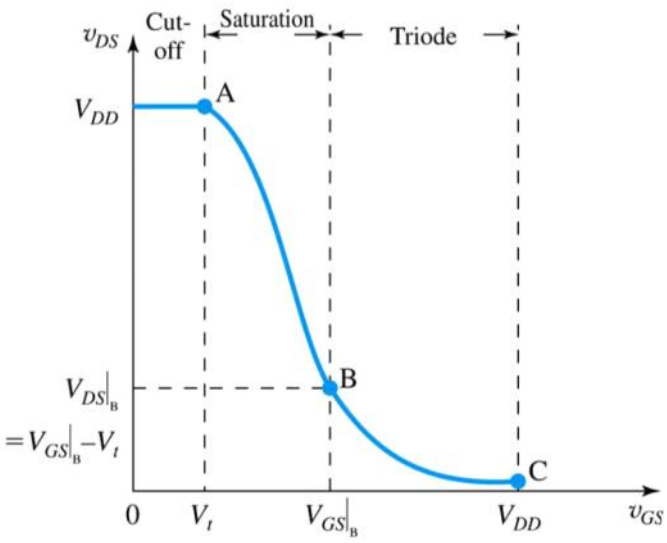
NMOS Inverter

Monday, February 14, 2022 12:03 PM

Def For the NMOS circuit:



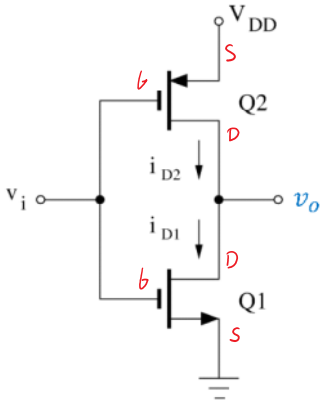
The transfer function:



CMOS Inverter

Monday, February 14, 2022 12:10 PM

Def Replacing the resistor in the NMOS inverter with a PMOS:



where:

GS1 KVL: $v_{GS1} = v_i$

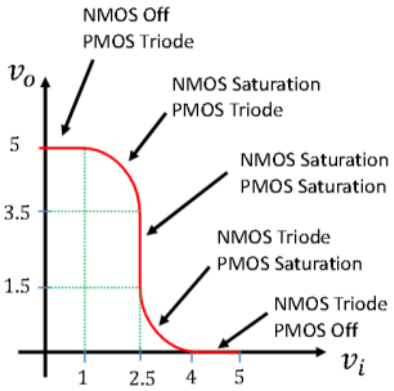
GS2 KVL: $V_{DD} = v_{SG2} + v_i$

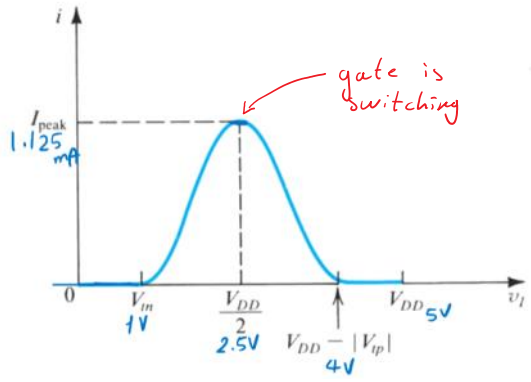
DS1&2 KVL: $V_{DD} = v_{SD2} + v_{DS1}$

KCL: $i_{D1} = i_{D2}$

$v_o = v_{DS1} = V_{DD} - v_{SD2}$

The transfer function of the inverter are: (assuming $k_n = k_p$ and $V_{tn} = V_{tp}$)



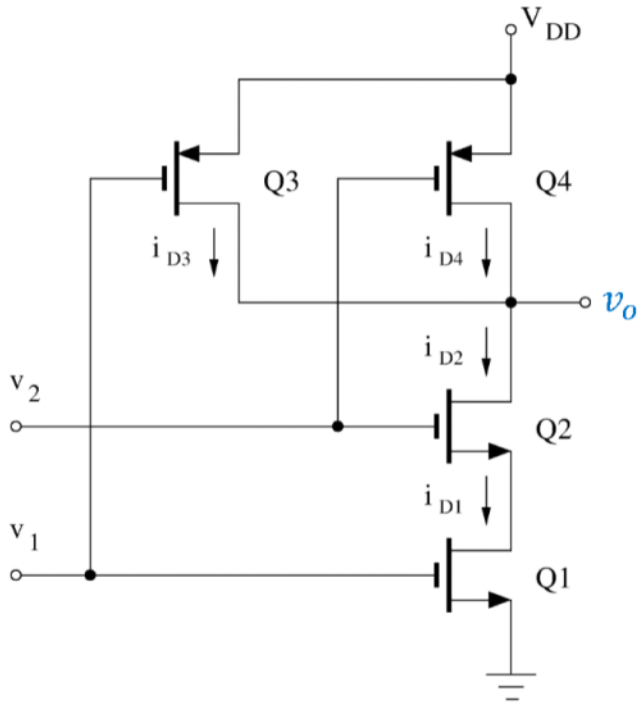


CMOS NAND Gate

Tuesday, February 15, 2022 6:15 PM

Truth Table

$v_1 = 0$	$v_2 = 0$:	$v_o = V_{DD}$
$v_1 = 0$	$v_2 = V_{DD}$:	$v_o = V_{DD}$
$v_1 = V_{DD}$	$v_2 = 0$:	$v_o = V_{DD}$
$v_1 = V_{DD}$	$v_2 = V_{DD}$:	$v_o = 0$



when gate is 0:

NMOS: off

PMOS: in triode

when gate is V_{DD}

NMOS: in triode

PMOS: off

Transistor Amplifiers

Tuesday, February 22, 2022 5:49 PM

Def We can design a linear amplifier using BJT or MOSFETs

The transfer function: $\frac{V_o}{V_i}$ must be constant and is the voltage gain

MOSFET:

When a MOSFET is in saturation, its transfer function looks linear but shifted

While the input signal is within the MOSFET's saturation region, it can be linearly amplified.

MOSFET Bias and Small Signal Response

Thursday, February 24, 2022 5:38 PM

Def Given some MOSFET amplifier, if $v_{gs} \ll 2(V_{GS} - V_t)$ then Small Signal Condition is satisfied.

then: $i_D \approx I_D + i_d \approx$ Bias Response + Signal Response

where: $I_D = \frac{1}{2} k (V_{GS} - V_t)^2$ and $i_d = k(V_{GS} - V_t) \cdot v_{gs}$

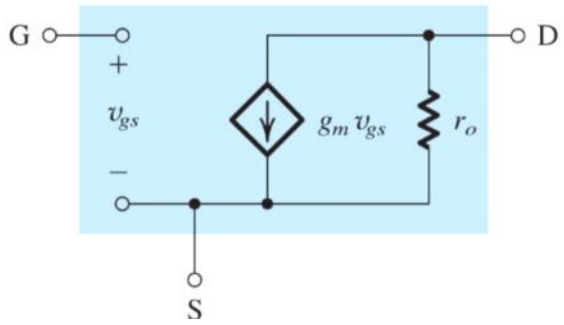
then the MOSFET transconductance $g_m = \frac{i_d}{v_{gs}} = \frac{2 I_D}{V_{ov}} = k \cdot V_{ov}$

Def Solving for the Bias Response:

1) Zero all signal sources. (voltage = short, current = open)
2) Set capacitors to open circuit. Set inductors to short circuits
3) Solve the circuit to find V_{DS}, V_{GS}, I_D, etc.

Def Solving for the Signal Response:

1) Zero all DC sources. (Voltage = short, Current = open)
2) Set the MOSFET to the following circuit: for both NMOS and PMOS



where $g_m = \frac{2 I_D}{V_{ov}} = k \cdot V_{ov}$

$r_o \approx \frac{1}{\lambda I_D}$

and $i_d = g_m v_{gs} + \frac{V_{ds}}{r_o} = g_m v_{gs} + V_{ds} \lambda I_D$

3) Set capacitors to short circuit. Set inductors to open circuit. Unless a frequency analysis is performed
4) Solve the circuit to find V_{ds}, v_{gs}, i_d, etc.

BJT Bias and Small Signal Response

Sunday, February 27, 2022 6:14 PM

Def Given that small signal is satisfied, we can use small signal approximation:

$i_C = I_C + i_c$: total output current is bias + signal

$g_m = \frac{I_C}{V_T}$

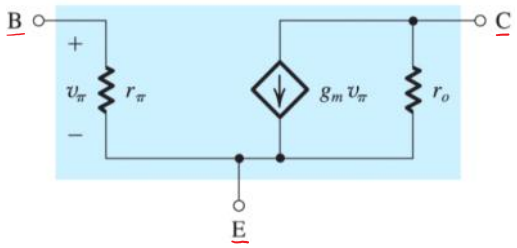
Def Solving the bias circuit: same as MOSFET.

Zero signal sources and solve for I_C

Def Solving the signal circuit:

1) Zero all DC sources. (Voltage = short, Current = open)

2) Set the BJT to the following circuit: for both PNP and NPN



where: $g_m = \frac{I_C}{V_T}$, $r_o = \frac{V_A}{I_C}$, $r_\pi = \frac{\beta}{g_m} = \frac{V_T}{I_B}$

if $V_A = \infty$ or $\lambda = 0$ (ignore early effect), $r_o = \infty$

3) Set capacitors to short circuit. Set inductors to open circuit.
Unless a frequency analysis is performed

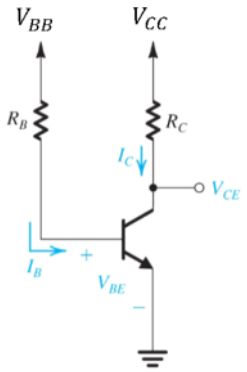
4) Solve the circuit to find V_{ds}, V_{gs}, i_d, etc.

BJT Amplifier Biasing

Tuesday, March 1, 2022 5:24 PM

Idea: for a BJT to act as a linear amplifier, we want the BJT to operate in the active region. Thus we want to DC bias the BJT.

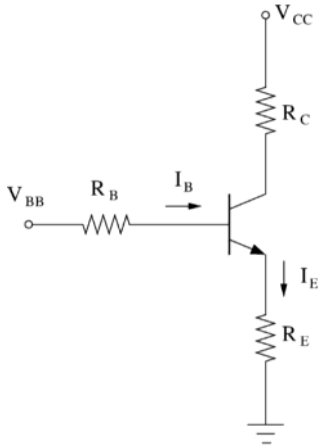
Types of Biasing: BJT Fixed Bias



$$I_B = \frac{V_{BB} - V_{BE}}{R_B}, \quad I_C = \beta I_B$$

Problem: Biasing depends heavily on β or V_{BE}

BJT Bias with Emitter Degeneration:



$$V_{BB} = R_B I_B + V_{BE} + R_E I_E$$

if $R_B << (\beta + 1) R_E$

then: $V_{BB} - V_{BE} \approx I_E R_E$

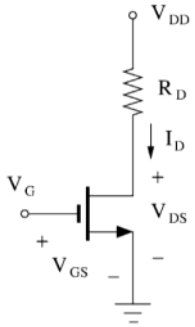
$$I_C \approx I_E \approx \frac{V_{BB} - V_{BE}}{R_E}$$

MOSFET Amplifier Biasing

Tuesday, March 1, 2022 5:38 PM

Idea: For a MOSFET to be a linear amplifier, we want it to operate in saturation.

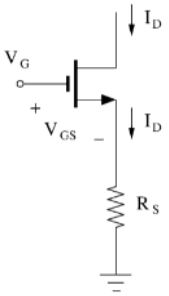
Types of MOSFET Biasing: MOSFET Fixed Bias:



$V_{DS} = V_{DD} - I_D R_D$ and $I_D = 0.5\,k\,(V_{GS} - V_T)^2$

problem: Biasing depends heavily on β or V_{GS}

MOSFET Source Degeneration Bias



$V_{DS} = V_b - I_D R_S$ and $I_D = 0.5\,k\,(V_{GS} - V_T)^2$

Transistor Amplifier Configurations

Thursday, March 3, 2022 5:01 PM

Def Transistor amplifiers can be represented as 2-port networks:

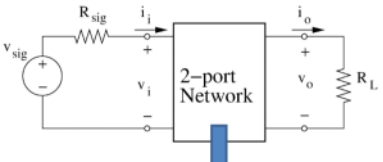
Voltage Gain of the Circuit: $A = \frac{v_o}{v_{sig}}$

Voltage Gain of the Amplifier: $A_v = \frac{v_o}{v_i}$

Open-loop Gain: $A_{vo} = \left.\frac{v_o}{v_i}\right|_{R_L \to \infty}$

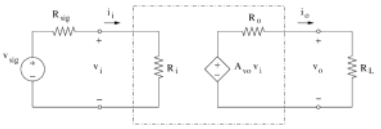
Input Resistance: $R_i = \frac{v_i}{i}$

Output Resistance of Amplifier: $R_o = -\left.\frac{v_o}{i_o}\right|_{v_i = 0}$

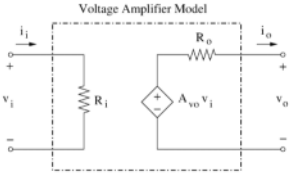


Overall Gain:

$$A = \frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}} \times \frac{v_o}{v_i} = \frac{R_i}{R_i + R_{sig}} A_v$$



Voltage Amplifier Model



$$\frac{v_i}{v_{sig}} = \frac{R_i}{R_i + R_{sig}}$$

Value of R_i is important.

- For $R_i >> R_{sig}$, $v_i \approx v_{sig}$
- For $R_i = R_{sig}$, $v_i = 0.5\ v_{sig}$
- For $R_i << R_{sig}$, $v_i \approx 0$

Prefer "large" R_i

$$A_v = \frac{v_o}{v_i} = \frac{R_L}{R_L + R_o} A_{vo}$$

A_{vo} is the maximum possible gain of the amplifier.

Value of R_o is important.

- For $R_o << R_L$, $A_v \approx A_{vo}$
- For $R_o = R_L$, $A_v = 0.5\ A_{vo}$
- For $R_o >> R_L$, $A_v \approx 0$

Prefer "small" R_o

Def There are a few configurations for BJT amplifier circuits

Common Collector: input applied at the base
output taken at the emitter

Common Emitter: input applied at the base
output taken at the collector

Common Base: input applied at the emitter
output taken at the collector

Def There are a few configurations for MOSFET amplifier circuits:

Common Drain: input applied at Gate
output taken at Source

Common Source: input applied at Gate
output taken at Drain

Common Gate: input applied at Source
output applied at Drain